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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,347	01/15/2002	Gurtej S. Sandhu	MI22-1897	7532

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EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	**PAPER NUMBER**
2813	
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06/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/050,347	SANDHU ET AL.	
	Examiner	Art Unit	
	Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This case has been REVIEWED and allowability is hereby withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 29 is rejected under 35 U.S.C. 102(b) as being anticipated by Holloway ('249).

The Holloway reference discloses a method of forming a transistor (MOSFET see Col.1, line: 1), comprising:

Forming a gate oxide layer over a semiconductor substrate (See Col.2, lines: 54-55, the gate oxide layer comprising silicon dioxide (See col.2, line: 11);

The gate oxide layer having an upper oxide-comprising surface and a lower oxide comprising surface (See Col.2, liens: 23-25 which discloses an upper surface and that a lower surface is inherent to any layer because layers comprise an upper and lower surface);

Exposing the gate oxide layer to an activated nitrogen species from a nitrogen containing plasma (Col.2, lines: 62-63) to introduce nitrogen into the gate oxide layer and form a nitrogen enriched region, the nitrogen enriched region being only in an upper half of the gate oxide layer (see Col.2, lines:15-20 and 26-31, where depth is maintained to about 1nm of a 4 nm gate oxide yielding top $1/4^{th}$ of the layer);

Thermally annealing the nitrogen within the nitrogen-enriched region to bond at least a majority of the nitrogen to silicon proximate the nitrogen; the nitrogen enriched region remaining

confined to the upper half of the gate oxide layer during annealing (temperature is 650 degrees C which inherently anneals because it is a temperature above ambient, that forms oxynitride-implies silicon oxynitride –see Col.2, lines:23-32);

Forming a conductive layer on and in direct physical contact with the upper oxide comprising surface of the gate oxide layer (Col.1, line:20 and Col.3, lines:6-7); and

Forming source/drain regions within the semiconductor substrate; the source/drain regions being gatedly connected to one another by the conductive layer (Col.3, lines: 8-9 state that the MOSFET transistor is completed which implies source/drain regions in the substrate as evidenced by Millman page 242, figure 8-6(f) includes source and drain regions "p" that are connected through a channel by controlling the gate voltage as described in para 8-4)

It should be noted that the claim does not require sequentially annealing as stated in the Reasons for Allowance dated 10/4/06. While t is true that nitrogen must be present in order to form a bond, the Holloway reference teaches the nitrogen species is implanted while the gate oxide is at a high temp of 650 degrees C which causes that particular nitrogen to bond to the silicon (See Holloway Col.2, lines: 57-62 where silicon dioxide converted to an oxynitride implies silicon oxynitride). This implantation/annealing continues until the oxynitride layer is formed at the required depth (See Col.2, lines:3-8, thereby allowing the nitrogen species that are implanted first to be at an elevated temperature for a certain period of time during the implantation). It should be noted that the Applicant's annealing time is as short as 30 seconds for a temperature of 700 degrees C (see Applicant's specification page 7) and the Holloway reference method results are similar (silicon oxynitride) layer in the gate oxide.

In reference to claim 30, wherein the N-enriched region is formed only in the upper third of the gate oxide layer by the exposing (see Col.2, lines:15-20 and 26-31, where depth is maintained to about 1nm of a 4 nm gate oxide yielding top $1/4^{th}$ of the layer).

In reference to claim 31, wherein the N-enriched region is formed only in the upper third of the gate oxide layer by the exposing (see Col.2, lines:15-20 and 26-31, where depth is maintained to about 1nm of a 4 nm gate oxide yielding top $1/4^{th}$ of the layer); and remains confined to the upper third of the gate oxide layer during the annealing (temperature is 650 degrees C which inherently anneals because it is a temperature above ambient, that forms oxynitride-implies silicon oxynitride –see Col.2, lines:23-32).

In reference to claim 32 wherein the gate oxide layer is maintained at a temperature of less than 400 degrees during the exposing (Col.2, lines: 1-10).

In reference to claim 35 wherein the exposing occurs for a time of less than or equal to about 1 minute (Col.2, lines: 1-10).

In reference to claim 36, wherein the annealing comprises thermal processing at temperature of less than 1100 for a time of at least 3 seconds (Col.2, lines: 1-10).

In reference to claim 37 wherein the conductive layer is a first conductive layer and further comprising forming a second conductive layer over the first conductive layer (Col.1, lines: 15-30- the polysilicon gate may be divided into multiple layers).

In reference to claim 38, wherein the conductive layer is formed after annealing (Col.3, lines: 1-10).

In reference to claim 39 wherein the source/drains are formed after annealing (Col.3, lines: 1-10- as explained above, the S/D formation is part of the std practice of forming a MOSFET).

In reference to claim 40 wherein the conductive layer and source/drain regions are formed after the annealing (Col.3, lines: 1-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holloway ('249).

Holloway teaches the limitations of claim 29 as explained above however fails to explicitly teach:

In reference to claim 33 wherein the plasma is maintained with a power from about 500 to 5000 W during the exposing.

In reference to claim 34 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5mTorr to 10 mTorr during the exposing.

The selection of the wattage and pressure is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

Claims 29-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holloway in view of Millman Microelectronics.

As noted in the 102 rejection, the Holloway reference discloses a method of forming a transistor (MOSFET see Col.1, line: 1), comprising:

Forming a gate oxide layer over a semiconductor substrate (See Col.2, lines: 54-55, the gate oxide layer comprising silicon dioxide (See col.2, line: 11);

The gate oxide layer having an upper oxide-comprising surface and a lower oxide comprising surface (See Col.2, liens: 23-25 which discloses an upper surface and that a lower surface is inherent to any layer because layers comprise an upper and lower surface);

Exposing the gate oxide layer to an activated nitrogen species from a nitrogen containing plasma (Col.2, lines: 62-63) to introduce nitrogen into the gate oxide layer and form a nitrogen enriched region, the nitrogen enriched region being only in an upper half of the gate oxide layer (see Col.2, lines:15-20 and 26-31, where depth is maintained to about 1nm of a 4 nm gate oxide yielding top $1/4^{th}$ of the layer);

Thermally annealing the nitrogen within the nitrogen-enriched region to bond at least a majority of the nitrogen to silicon proximate the nitrogen; the nitrogen enriched region remaining confined to the upper half of the gate oxide layer during annealing (temperature is 650 degrees C which inherently anneals because it is a temperature above ambient, that forms oxynitride-implies silicon oxynitride –see Col.2, lines:23-32);

Forming a conductive layer on and in direct physical contact with the upper oxide comprising surface of the gate oxide layer (Col.1, line:20 and Col.3, lines:6-7); and

However, the reference does not explicitly state "Forming source/drain regions within the semiconductor substrate; the source/drain regions being gatedly connected to one another by the conductive layer" as required in claim 29.

Nevertheless the Millman reference teaches on page 242 as shown in figure 8-6(f), a MOSFET includes source and drain regions "p" that are connected through a channel by controlling the gate voltage as described in para 8-4.

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to have included source/drains in the substrate of the MOSFET that are gatedly connected to one another by the conductive gate electrode of the Holloway as taught by Millman because as the reference is silent on the details of the MOSFET source/drains, one of ordinary skill in the art would have been motivated to use any known configuration such as the one disclosed in Millman. It should be noted that the arguments concerning "sequentially" discussed in the proposed 102 rejection are also applicable.

In reference to claim 30, wherein the N-enriched region is formed only in the upper third of the gate oxide layer by the exposing (see Col.2, lines:15-20 and 26-31, where depth is maintained to about 1nm of a 4 nm gate oxide yielding top $1/4^{th}$ of the layer).

In reference to claim 31, wherein the N-enriched region is formed only in the upper third of the gate oxide layer by the exposing (see Col.2, lines:15-20 and 26-31, where depth is maintained to about 1nm of a 4 nm gate oxide yielding top $1/4^{th}$ of the layer); and remains confined to the upper third of the gate oxide layer during the annealing (temperature is 650 degrees C which inherently anneals because it is a temperature above ambient, that forms oxynitride-implies silicon oxynitride –see Col.2, lines:23-32).

In reference to claim 32 wherein the gate oxide layer is maintained at a temperature of less than 400 degrees during the exposing (Col.2, lines: 1-10).

Holloway and Millman teaches the limitations of claim 29 as explained above however fails to explicitly teach:

In reference to claim 33 wherein the plasma is maintained with a power from about 500 to 5000 W during the exposing.

In reference to claim 34 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5mTorr to 10 mTorr during the exposing.

The selection of the wattage and pressure is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

In reference to claim 35 wherein the exposing occurs for a time of less than or equal to about 1 minute (Col.2, lines: 1-10).

In reference to claim 36, wherein the annealing comprises thermal processing at temperature of less than 1100 for a time of at least 3 seconds (Col.2, lines: 1-10).

In reference to claim 37 wherein the conductive layer is a first conductive layer and further comprising forming a second conductive layer over the first conductive layer (Col.1, lines: 15-30- the polysilicon gate may be divided into multiple layers).

In reference to claim 38, wherein the conductive layer is formed after annealing (Col.3, lines: 1-10).

In reference to claim 39 wherein the source/drains are formed after annealing (Col.3, lines: 1-10- as explained above, the S/D formation is part of the std practice of forming a MOSFET).

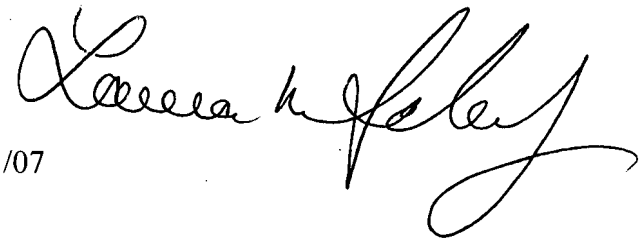
In reference to claim 40 wherein the conductive layer and source/drain regions are formed after the annealing (Col.3, lines: 1-10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Laura M Schillinger
Primary Examiner
Art Unit 2813

06/01/07